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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/014,243	12/11/2001	Renerus Antonius Van Den Heuvel	NL 000674	3083

7590

04/10/2003

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EXAMINER

MALDONADO, JULIO J

ART UNIT

PAPER NUMBER

2823

DATE MAILED: 04/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/014,243

Applicant(s)

VAN DEN HEUVEL, RENERUS
ANTONIUS

Examiner

Julio J. Maldonado

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 March 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 December 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 6.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

DETAILED ACTION

1. Applicant's cancellation to claim 9 is acknowledged.
2. Claims 1-8 are pending in this application.

Election/Restrictions

3. Applicant's election without traverse of claims 1-8 in Paper No. 9 is acknowledged.

Drawings

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: page 5, lines 27-31 makes reference to reference characters "20", "21" and "22" in Fig.1 which are not on the drawings; page 6, lines 1-12 makes reference to reference characters "3" and "25" in Fig.1 which are not on the drawings. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

Content of Specification

- (a) Title of the Invention: See 37 CFR 1.72(a) and MPEP § 606. The title of the invention should be placed at the top of the first page of the specification unless the title is provided in an application data sheet. The title of the invention should be brief but technically accurate and descriptive, preferably from two to seven words may not contain more than 500 characters.
- (b) Cross-References to Related Applications: See 37 CFR 1.78 and MPEP § 201.11.

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- (c) Statement Regarding Federally Sponsored Research and Development:
See MPEP § 310.
- (d) Incorporation-By-Reference Of Material Submitted On a Compact Disc:
The specification is required to include an incorporation-by-reference of electronic documents that are to become part of the permanent United States Patent and Trademark Office records in the file of a patent application. See 37 CFR 1.52(e) and MPEP § 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text were permitted as electronic documents on compact discs beginning on September 8, 2000.

Or alternatively, Reference to a "Microfiche Appendix": See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.
- (e) Background of the Invention: See MPEP § 608.01(c). The specification should set forth the Background of the Invention in two parts:
 - (1) Field of the Invention: A statement of the field of art to which the invention pertains. This statement may include a paraphrasing of the applicable U.S. patent classification definitions of the subject matter of the claimed invention. This item may also be titled "Technical Field."
 - (2) Description of the Related Art including information disclosed under 37 CFR 1.97 and 37 CFR 1.98: A description of the related art known to the applicant and including, if applicable, references to specific related art and problems involved in the prior art which are solved by the applicant's invention. This item may also be titled "Background Art."
- (f) Brief Summary of the Invention: See MPEP § 608.01(d). A brief summary or general statement of the invention as set forth in 37 CFR 1.73. The summary is separate and distinct from the abstract and is directed toward the invention rather than the disclosure as a whole. The summary may point out the advantages of the invention or how it solves problems previously existent in the prior art (and preferably indicated in the Background of the Invention). In chemical cases it should point out in general terms the utility of the invention. If possible, the nature and gist of the invention or the inventive concept should be set forth. Objects of the invention should be treated briefly and only to the extent that they contribute to an understanding of the invention.

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- (g) Brief Description of the Several Views of the Drawing(s): See MPEP § 608.01(f). A reference to and brief description of the drawing(s) as set forth in 37 CFR 1.74.
- (h) Detailed Description of the Invention: See MPEP § 608.01(g). A description of the preferred embodiment(s) of the invention as required in 37 CFR 1.71. The description should be as short and specific as is necessary to describe the invention adequately and accurately. Where elements or groups of elements, compounds, and processes, which are conventional and generally widely known in the field of the invention described and their exact nature or type is not necessary for an understanding and use of the invention by a person skilled in the art, they should not be described in detail. However, where particularly complicated subject matter is involved or where the elements, compounds, or processes may not be commonly or widely known in the field, the specification should refer to another patent or readily available publication which adequately describes the subject matter.
- (i) Claim or Claims: See 37 CFR 1.75 and MPEP § 608.01(m). The claim or claims must commence on separate sheet (37 CFR 1.52(b)). Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation. There may be plural indentations to further segregate subcombinations or related steps. See 37 CFR 1.75 and MPEP § 608.01(i)-(p).
- (j) Abstract of the Disclosure: See MPEP § 608.01(f). A brief narrative of the disclosure as a whole in a single paragraph of 150 words or less commencing on a separate sheet following the claims. In an international application which has entered the national stage (37 CFR 1.491(b)), the applicant need not submit an abstract commencing on a separate sheet if an abstract was published with the international application under PCT Article 21. The abstract that appears on the cover page of the pamphlet published by the International Bureau (IB) of the World Intellectual Property Organization (WIPO) is the abstract that will be used by the USPTO. See MPEP § 1893.03(e).
- (k) Sequence Listing. See 37 CFR 1.821-1.825 and MPEP §§ 2421-2431. The requirement for a sequence listing applies to all sequences disclosed in a given application, whether the sequences are claimed or not. See MPEP § 2421.02.

Claim Objections

5. Claims 1 and 2 are objected to because of the following informalities: in claim 1, the term "characterised" should be replaced with "characterized". Appropriate correction is required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1-6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jin et al. (U.S. 6,350,665 B1) in view of Odake et al. (U.S. 6,030,869) and Fulford, Jr. et al. (U.S. 5,789,780).

In reference to claims 1, 6 and 8, Jin et al. (Figs.3-4D) in a related method to form source and drain junctions in a semiconductor device comprising having one or more passive components integrated into a semiconductor body (402) teach a semiconductor device containing a field effect transistor with a gate electrode (404), a source region (412-0) and a drain region (412-1), wherein the source region (424-0) and the drain region (424-1) are formed, in the semiconductor body (402), on both sides of the gate electrode (404) and a part (424-1) of the drain region (424-1) bordering the gate electrode (404) is provided with a lower doping concentration, and wherein a silicon nitride spacer (408) is produced on both sides of the gate electrode (404), characterized in that for the formation of the drain region (412-1) and the lowly doped

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part (421-4) thereof, the drain region (412-1) being formed at a distance from the gate electrode (404) that is larger than the width of the spacer (408) (column 7, line 46 – column 9, line 45).

Jin et al. fail to teach forming a gate oxide over the surface of the semiconductor body; and forming the source and drain regions with two additional mask in layers deposited on the surface of the semiconductor body. However, Odake et al. (Figs.2a-3a) in a related method to form source and drain regions in a semiconductor device teach forming a gate oxide (3)² over a semiconductor body (1); and forming source and drain regions with two masking layers (8, 13) deposited on the surface of a semiconductor body (1) (column 6, line 61 – column 7, line 67). Therefore, it would have been obvious to combine the teachings of Odake et al. and Jin et al. to enable the formation of a gate oxide and source and drain regions as taught by Odake et al.

The combined teachings of Jin et al. and Odake et al. fail to teach forming the spacers from a material that can be selectively etched with respect to the gate oxide layer. However, Fulford, Jr. et al. (Figs.3A-3D) in a related method to form a semiconductor device with detached source regions teach forming the spacers from a material that can be selectively etched with respect to the gate oxide layer (column 17, lines 19 – 43). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teachings of Fulford, Jr. et al. with the combined teachings of Jin et al. and Odake et al. to enable spacers with an etch selectivity to be formed.

In reference to claims 2-5, Jin et al., Odake et al. and Fulford Jr. et al. teach wherein for the formation of the lowly doped part of the drain region a first masking layer

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extending so far as to be on the gate electrode is produced on the side of the gate electrode of the source region to be formed on the surface of the semiconductor body, and a second masking layer extending from the gate electrode up to the drain region to be formed is produced on the surface of the semiconductor body (Otake et al., Figs. 2c and 3a); wherein at the location of the source region and the drain region the gate oxide layer is provided with an aperture and that at the location of said aperture the gate electrode, the source region and the drain region are provided with a metal layer, comprising a silicide (Jin et al., column 9, lines 25 – 35); wherein on the gate electrode an isolating layer is deposited, on which a shielding electrode is produced at the location of the gate electrode (Otake et al., column 6, line 61 – column 7, line 5). The combined teachings of Jin et al., Otake et al. and Fulford Jr. et al. also teach displacing the drain region to increase the transistor tolerance to drain voltage breakdown (Fulford Jr. et al., column 3, lines 23 – 27).

The combined teachings of Jin et al., Otake et al. and Fulford Jr. et al. fail to teach converting the metal layer into a silicide layer with the aid of the underlying silicon and wherein the distance from the drain region to the gate electrode is chosen between 1 and 4 μm . However, the examiner takes official notice that the process of converting a metal layer into a silicide layer is common practice within the scope of one of ordinary skill in the art and therefore it would have been obvious to use the underlying silicon layer to convert a metal layer to a metal silicide layer. Also, the examiner takes official notice that the dimensional range of the drain region to the gate region involves routine optimization within the scope of one of ordinary skill in the art. One of ordinary skill in

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the art would have been led to the recited drain region size through routine experimentation within the teachings of the process of Jin et al., Odake et al. and Fulford Jr. et al. to achieve a desired property of the transistor device

8. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jin et al. ('665 B1) in view of Odake et al. ('869) and Fulford, Jr. et al. ('780) as applied to claims 1-6 above, and further in view of Ishimaru et al. (U.S. 6,365,472 B1).

The combined teachings of Jin et al., Odake et al. and Fulford Jr. et al. substantially teach all aspects of the invention but fail to teach wherein the spacers are formed of a layer of silicon nitride on which a layer of polycrystalline silicon is deposited. However, Ishimaru et al. in a related method to form a transistor device teach forming a first spacer (6) over the sidewalls of a gate electrode (3); and forming a layer of polycrystalline silicon (7) over the silicon nitride sidewall (6) (column 4, line 58 – column 5, line 16). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ishimaru et al. in the transistor device of Jin et al., Odake et al. and Fulford Jr. et al. to enable the formation of the polycrystalline silicon layer over the silicon nitride spacer as taught by Ishimaru et al., and furthermore to protect the substrate from implantation steps, thus reducing damages to the underlying substrate and reducing current leakage (column 2, lines 42 – 50).

Conclusion


9. Papers related to this application may be submitted directly to Art Unit 2823 by facsimile transmission. Papers should be faxed to Art Unit 2823 via the Art Unit 2823

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Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2823 Fax Center number is **(703) 305-3432**. The Art Unit 2823 Fax Center is to be used only for papers related to Art Unit 2823 applications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Julio J. Maldonado** at **(703) 306-0098** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via julio.maldonado@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (703) 306-2794.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.


JMR
4/4/03


George Fourson
Primary Examiner